

User's Guide - DDR3 Compliance Test

Rev. 1, June 2010

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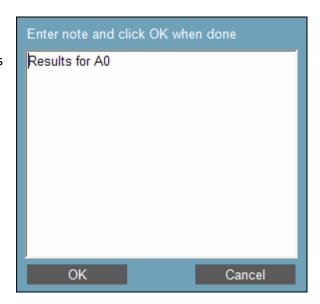
1 Introduction

The DDR3 Compliance Test uses the *JEDEC JESD 79-3C DDR3 SDRAM Standard*, *November 2008* as a reference. There are four data rates for DDR3: 800 Mbps, 1066 Mbps, 1333 Mbps, and 1600 Mbps. ¹ The parameters and values tested vary for each of the four rates, so there are four TestScripts provided as part of the DDR3 Compliance Test. The operator should choose the appropriate TestScript for the data rate of the DUT.

Some dialogs, such as the **Individual Results Dialog**, occur commonly in the course of testing. Descriptions of such dialogs are provided in **Appendix A**, and are referred to in the course of the test descriptions. To find out what test will perform the measurement for a particular parameter, consult **Appendix B**.

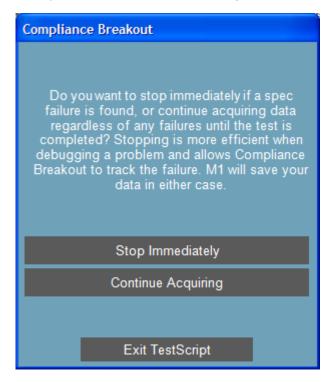


Where possible, the title of the test indicates which signal is being tested. In some cases, however, a sequence of signals, such as address lines A0 through A15, will be tested. In these cases, when the Individual Test Results Dialog appears, the operator should use the Add Note button to bring up the dialog on the right. The operator should enter a note indicating the signal that was tested; this note will be included in the final report for ease of identifying any signals that fail the testing.



All tests start with two dialogs that tell what version of the JEDEC specification is being used, and the version of M1 OT that is needed to successfully run the Compliance Test. At the end of the test, the results of all testing may be saved to a file for documentation.

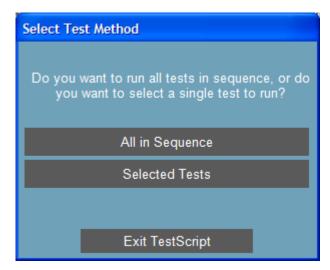
The operator will then see this dialog:



This dialog gives the option of either stopping when the first out-of-spec measurement is found, or continuing the test until the proper number for events has been detected. Selecting Continue Acquiring will make it more likely that all possible error conditions are found, since it is possible that not all out-of-spec conditions will happen at the same time. However, selecting Stop Immediately will ensure that the Compliance Breakout feature of M1 will be available to analyze the problematic waveform. The operator should make the selection based upon which scenario is appropriate. The mode selected will be applied to all tests that are conducted during this execution of the Compliance Test.



After these dialogs have appeared, the operator will see the Select Test Method dialog:



Operator Action: Click on All in Sequence to run all DDR3 Tests, or Selected Tests to select a single test to run. If All in Sequence is chosen, the operator will be given the option of running each test, or skipping the test.

1.1 Probes Needed

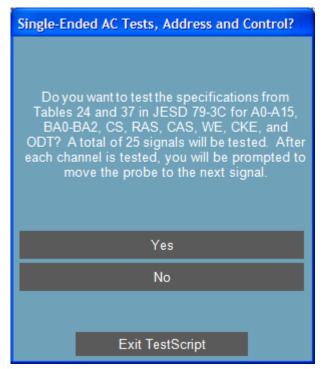
The operator will need two single-ended probes and two differential probes for these tests.



2 All in Sequence

2.1 Single-Ended AC Input Tests, Address and Control

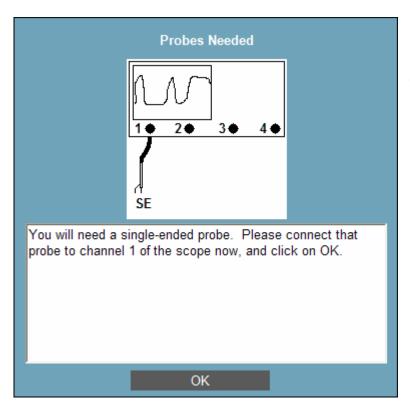
The operator will see this dialog:



Operator Action: Click Yes to perform the tests, or No to skip the tests. This document will assume that the operator clicks Yes. Otherwise, skip to Section 2.2, Single-Ended AC Tests, Data, Strobe, and Mask.



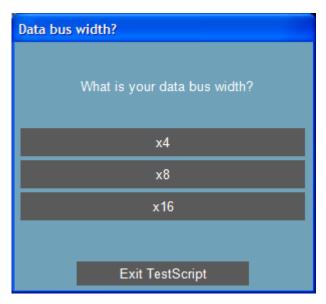
This dialog will appear:



Operator Action: Attach a single-ended probe to Channel 1. Probe A0 with the single-ended probe.

Testing will proceed, with the operator being prompted to probe lines AO-A15, BAO-BA2, CS, RAS, CAS, WE, CKE, and ODT. When the Individual Test Results dialog comes up for each line and all buttons are enabled, use Add Note to record which line was tested.

When these lines have been tested, the operator will see this dialog:



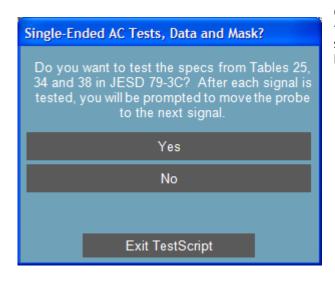
Operator Action: Click on the button that correctly indicates the data bus width for the DUT.

The tests that follow will differ only slightly, depending on the data bus width.



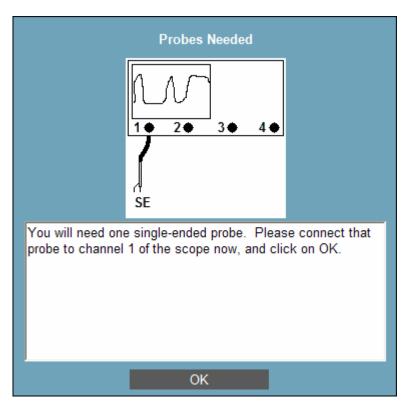
2.2 Single-Ended AC Tests, Data and Mask

The operator will see this dialog:



Operator Action: Click on Yes to conduct the tests. If the operator clicks on No to skip the tests, skip to Section 2.3, Differential Input Tests.

The operator will see this dialog:

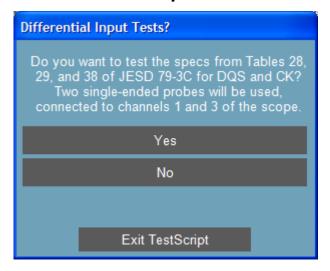


Operator Action: Connect a single-ended probe to Channel 1. Probe DQ0 with the probe attached Channel 1. Click on OK.

Lines DQ0-DQn (where n depends on the data bus width) and DM will be tested. The operator will be prompted when it is time to move the probe. When the Individual Test Results dialog comes up for each line and all buttons are enabled, use Add Note to record which line was tested.

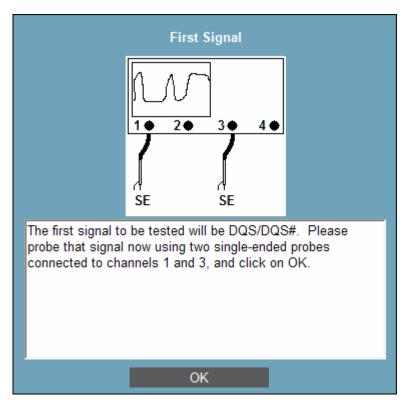


2.3 Differential Input Tests



Operator Action: Click on Yes to conduct the tests. If the operator clicks on No to skip the tests, skip to Section 2.4, Differential Output Tests.

The operator will see this dialog:



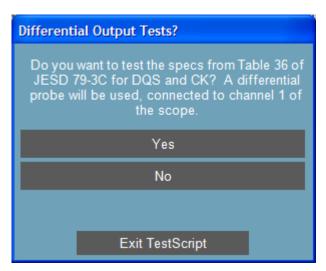
Operator Action: Connect two single-ended probes to Channels 1 and 3 of the scope. Probe DQS/DQS# with the two probes. Click on OK.

When testing of **DQS/DQS#** is finished, the operator will be prompted to move the probes to **CK/CK#**.



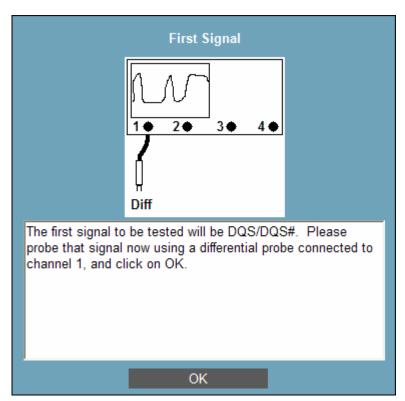
2.4 Differential Output Tests

After the **Differential Input** tests are complete, the operator will see:



Operator Action: Click on Yes to conduct the tests. If the operator clicks on No to skip the tests, skip to Section 2.5, Data Timing.

The operator will see this dialog:



Operator Action: Connect a differential probe to Channel 1 of the scope, and probe DQS/DQS# with it. Click on OK.

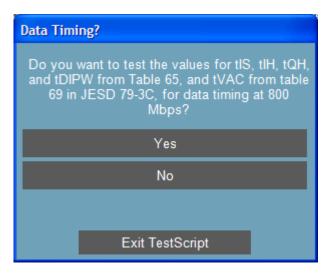
If the Data Bus Width is 16, LDQS/LDQS# will be tested first, then the operator will be prompted to move the probes to UDQS/UDQS#.

After DQS/LDQS/UDQS testing is done, the operator will be prompted to probe CK/CK#.



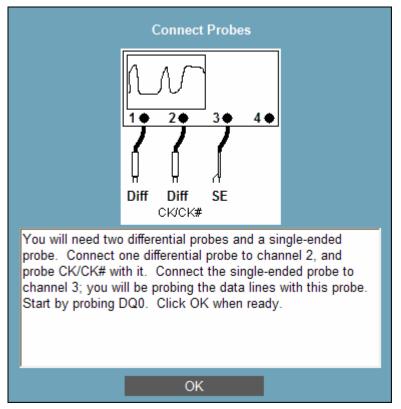
2.5 Data Timing

The operator will see this dialog:



Operator Action: Click on Yes to conduct the tests. If the operator clicks on No to skip the tests, skip to the Section 2.6, Data Strobe Timing.

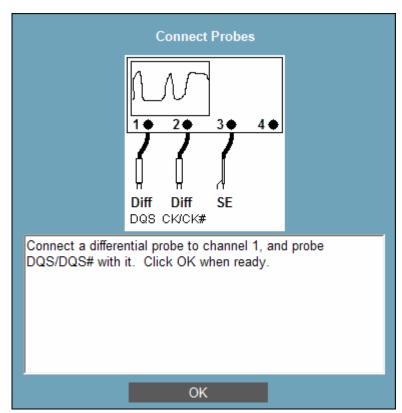
The operator will see this dialog:



Operator Action: Connect a differential probe to Channel 1. Connect another differential probe to Channel 2 and probe CK/CK# with it. Connect a single-ended probe to Channel 3, and probe DQ0 with it. Click on OK.



The operator will see this dialog:



Operator Action: Probe DQS/DQS# with the differential probe attached to Channel 1. If the data bus width is 16, the operator will be prompted to probe LDQS/LDQS# instead. Click on OK.

The operator will be prompted to probe **DQ0** with the **single-ended** probe. *If* the data bus width is 16, the operator will be prompted to probe **DQL0** instead.

Lines DQ0-DQn (where n depends on the data bus width) will be tested. The operator will be prompted when it is time to move the probe. When the Individual Test Results dialog comes up for each line and all buttons are enabled, use Add Note to record which line was tested.

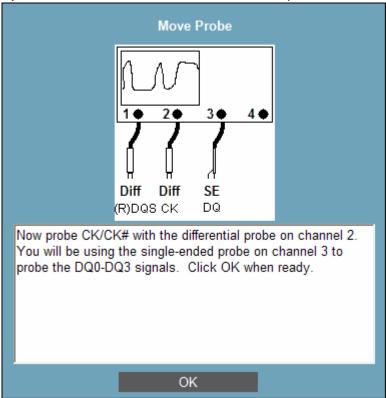
If the data bus width is 16,

DQLO-DQL7 will be tested. Then the operator will be prompted to move the **differential** probe on Channel 1 to **UDQS** for testing of **DQU0-DQU7**.



The operator will see the dialog:

Operator Action: Confirm that the differential probe on Channel 2 is probing CK/CK#. Click on OK.



The operator will be prompted to probe **DQ0** with the **single-ended** probe. *If* the data bus width is 16, the operator will be prompted to probe **DQL0** instead.

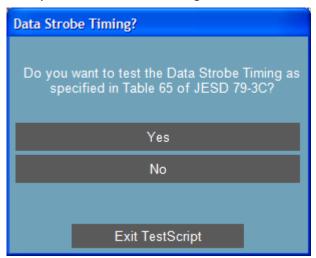
Lines DQ0-DQn (where n depends on the data bus width) will be tested. The operator will be prompted when it is time to move the probe. When the Individual Test Results dialog comes up for each line and all buttons are enabled, use Add Note to record which line was tested.

If the data bus width is 16, DQL0-DQL7 and DQU0-DQU7 will be tested.



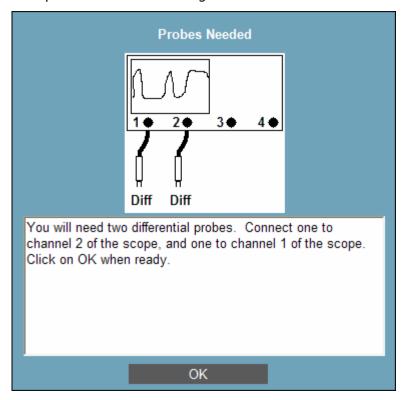
2.6 Data Strobe Timing

The operator will see this dialog:



Operator Action: Click Yes to perform the test, or No to skip the test. This document will assume that the operator clicks Yes. Otherwise, skip to Section 2.7, Clock Tests.

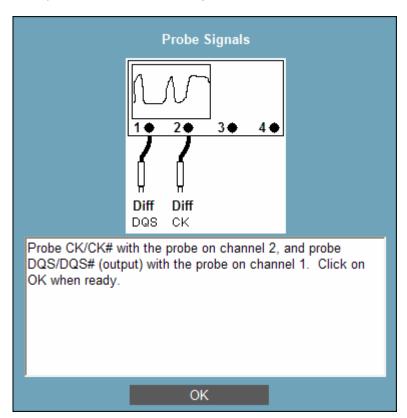
The operator will see this dialog:



Operator Action: Connect differential probes to Channels 1 and 2 of the scope. Click on OK.



The operator will see this dialog:



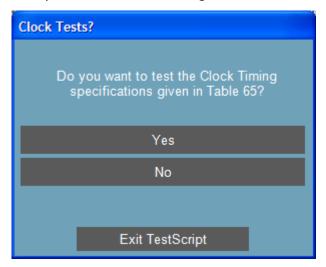
Operator Action: Probe CK/CK# with the differential probe on Channel 2, and probe DQS/DQS# (output) with the probe on Channel 1. Click on OK.

If the data bus width is 16, the operator will be prompted to probe LDQS/LDQS# (output), the test will be performed, then the operator will be prompted to probe UDQS/UDQS# (output).

After the output tests are performed, the operator will be prompted to probe the **DQS** input.

2.7 Clock Tests

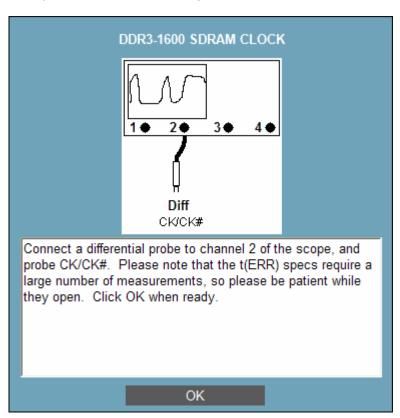
The operator will see this dialog box:



Operator Action: Click Yes to perform the test, or No to skip the test. This document will assume that the operator clicks Yes. Otherwise, skip to Section 2.8, Command and Address Timing.



The operator will see this dialog box:



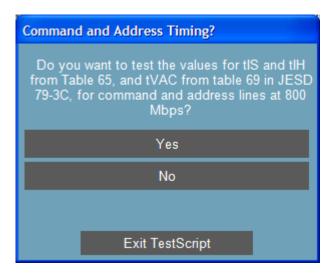
Operator Action: Connect a differential probe to Channel 2 of the scope. Probe CK/CK# with the differential probe. Click OK.

M1 will perform a series of acquisitions. While the acquisitions are being made, the Individual Test Results dialog will be displayed; see Appendix A for a description of the dialog. The operator should not click on anything until all buttons are enabled. Once all buttons are enabled, click on Close and Continue.



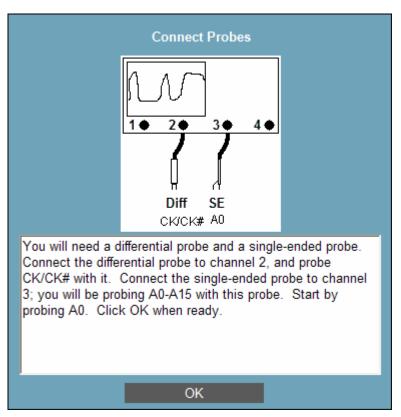
2.8 Command and Address Timing

This dialog will appear:



Operator Action: Click on **Yes** to conduct the tests. If the operator clicks on **No** to skip the tests, the testing for DDR3 is complete.

The operator will see this dialog:



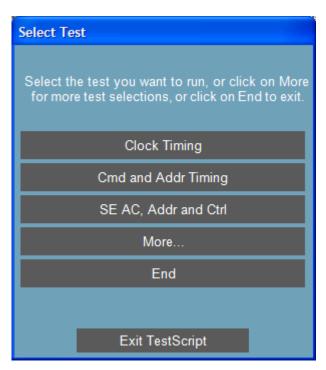
Operator Action: Connect a differential probe to Channel 2 of the scope. Probe CK/CK# with the differential probe. Connect a single-ended probe to Channel 3 of the scope. Probe A0 with the single-ended probe. Click OK.



Testing will continue, with prompting to move the single-ended probe to the next address line. Each time the Individual Test Results dialog appears, and all of its buttons are enabled, the operator should enter a note to indicate which address line was tested. When the last address line has been probed (A15), the operator will be prompted to move the probe to the "next" address line; this dialog should be ignored, as it will be followed by a prompt to move the single-ended probe to CS0. Testing will continue, with prompting to move the single-ended probe to CS1, CS2, CS3, RAS, CAS, and WE. Again, the Add Note button on the Individual Test Results dialog should be used to indicate which control line was tested.

3 Selected Tests

The operator will see this dialog:



Operator Action: If the desired test is shown on this dialog, the operator should click on the test and see the instructions in the appropriate section above; it may help to refer to the Table of Contents. If the desired test is not shown, the operator should click on More...



Clicking on More... will display this dialog:

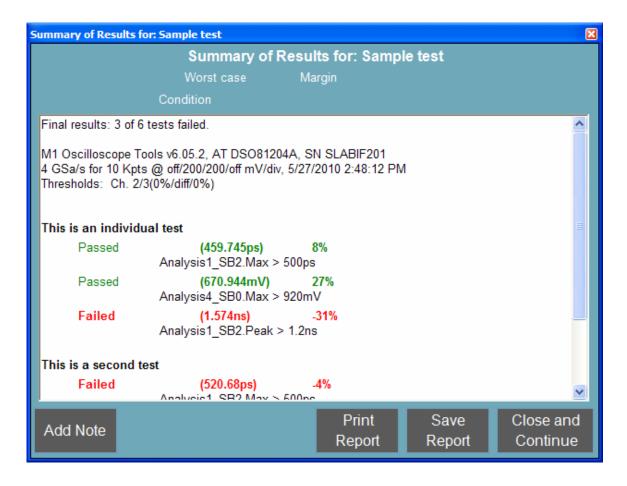


Operator Action: If the desired test is shown on this dialog, the operator should click on the test and see the instructions in the appropriate section above; it may help to refer to the Table of Contents. The operator should click on End to exit the Compliance Test.



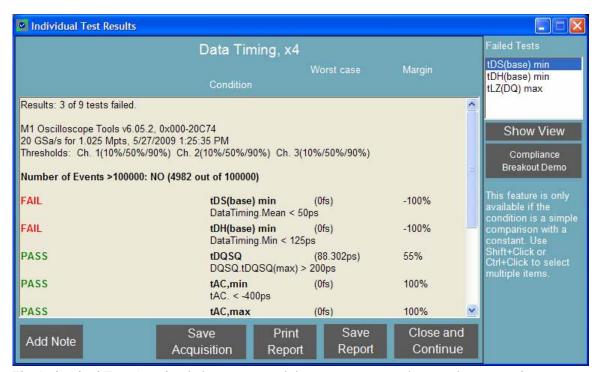
4 Testing Complete

When testing is complete, a summary of all tests run will be presented in a dialog. At this time the operator should use **Add Note** to add any notes regarding any unexpected events during the test, and click on **Save Report** to save the results of the testing in an appropriate place and format.





Appendix A – Individual Test Results Dialog



The **Individual Test Results** dialog appears while acquisitions are being taken to perform a test. Some of the buttons on the bottom will be disabled while testing is being done; when they are all enabled, the test has completed. The operator should not take any action if any of the buttons on the bottom are disabled.

The main text display shows a summary line telling the overall results, as well as information about the scope being used, the acquisition settings of the scope, and the time the acquisitions started. The remainder of the main text display tells the status of each condition being tested (PASS or FAIL).

The Add Note button brings up a dialog that will let the operator enter a note about the test. It is recommended that the operator add a note for each signal that is tested, so that failure or success may be associated with the correct signal for later analysis. For instance, if lines DQ0-DQ15 are being tested, the text "DQ0", "DQ1", etc. would be entered as each data line was tested. These notes will automatically be stored with the test results for the final report; it is not necessary to save each individual test result separately.

If none of the tests failed, the right-hand portion of the dialog ("Failed Tests") will not be visible.



Appendix B – Parameters Tested

This appendix lists the parameters tested by this Compliance Test, in which section the parameter is tested, and which signal lines are tested. Section numbers refer to section numbers in this document.

Parameter	Tested in Section	Signals Tested
JIT(cc) max	2.7 Clock Tests	CK/CK#
JIT(per) min, max	2.7 Clock Tests	CK/CK#
Overshoot area	2.1 Single-Ended AC Input Tests, Address and Control	A0-A15, BA0-BA2, CS, RAS, CAS, WE, CKE, ODT
Overshoot area	2.2 Single-Ended AC Tests, Data and Mask	DQ*, DM
Overshoot area	2.3 Differential Input Tests	DQS/DQS#, LDQS/LDQS#. UDQS/UDQS#, CK/CK#
Overshoot Peak	2.3 Differential Input Tests	DQS/DQS#, LDQS/LDQS#. UDQS/UDQS#, CK/CK#
SRQdiff Rise min, max	2.4 Differential Output Tests	DQS/DQS#, LDQS/LDQS#. UDQS/UDQS#, CK/CK#
SRQdiff Fall min, max	2.4 Differential Output Tests	DQS/DQS#, LDQS/LDQS#. UDQS/UDQS#, CK/CK#
SRQse min, max	2.5 Data Timing	DQ*
tCH(abs) min	2.7 Clock Tests	CK/CK#
tCH(avg) min, max	2.7 Clock Tests	CK/CK#
tCK(abs) min, max	2.7 Clock Tests	CK/CK#
tCK(avg) min, max	2.7 Clock Tests	CK/CK#
tCL(abs) min, max	2.7 Clock Tests	CK/CK#
tCL(avg) min, max	2.7 Clock Tests	CK/CK#
tDH(base) min	2.5 Data Timing	DQ*
tDIPW	2.5 Data Timing	DQ*



Parameter	Tested in Section	Signals Tested
tDQSCK min, max	2.6 Data Strobe Timing	DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# (output)
tDQSH min, max	2.6 Data Strobe Timing	DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# (input)
tDQSL min, max	2.6 Data Strobe Timing	DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# (input)
tDQSQ	2.5 Data Timing	DQ*
tDQSS min, max	2.6 Data Strobe Timing	DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# (input)
tDS(base) min	2.5 Data Timing	DQ*
tDSH	2.6 Data Strobe Timing	DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# (input, output)
tDSS	2.6 Data Strobe Timing	DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# (input, output)
tERR* min, max	2.7 Clock Tests	CK/CK#
tHZ(DQ)	2.5 Data Timing	DQ*
tHZ(DQS) max	2.6 Data Strobe Timing	DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# (input, output)
tIH(base) min	2.8 Command and Address Timing	A*, CS*, RAS, CAS, WE
tIS(base) min	2.8 Command and Address Timing	A*, CS*, RAS, CAS, WE
tIPW min	2.8 Command and Address Timing	A*, CS*, RAS, CAS, WE
tLZ(DQ) min, max	2.5 Data Timing	DQ*
tLZ(DQS) min, max	2.6 Data Strobe Timing	DQS/DQS#, LDQS/LDQS#,



Parameter	Tested in Section	Signals Tested
		UDQS/UDQS# (input, output)
tQH	2.5 Data Timing	DQ*
tQSH	2.6 Data Strobe Timing	DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# (output)
tQSL	2.6 Data Strobe Timing	DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# (output)
tRPRE min	2.6 Data Strobe Timing	DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# (input, output)
tRPST min	2.6 Data Strobe Timing	DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# (input, output)
tVAC	2.5 Data Timing	DQ*
tVAC min	2.8 Command and Address Timing	A*, CS*, RAS, CAS, WE
tWPRE min	2.6 Data Strobe Timing	DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# (input, output)
tWPST min	2.6 Data Strobe Timing	DQS/DQS#, LDQS/LDQS#, UDQS/UDQS# (input, output)
Undershoot area	2.1 Single-Ended AC Input Tests, Address and Control	A0-A15, BA0-BA2, CS, RAS, CAS, WE, CKE, ODT
Undershoot area	2.2 Single-Ended AC Tests, Data and Mask	DQ*, DM
Undershoot area	2.3 Differential Input Tests	DQS/DQS#, LDQS/LDQS#. UDQS/UDQS#, CK/CK#
Undershoot Peak	2.3 Differential Input Tests	DQS/DQS#, LDQS/LDQS#. UDQS/UDQS#, CK/CK#



Parameter	Tested in Section	Signals Tested
Vhigh	2.2 Single-Ended AC Tests, Data and Mask	DQ*, DM
VIH.CA(AC)	2.1 Single-Ended AC Input Tests, Address and Control	A0-A15, BA0-BA2, CS, RAS, CAS, WE, CKE, ODT
VIL.CA(AC)	2.1 Single-Ended AC Input Tests, Address and Control	A0-A15, BA0-BA2, CS, RAS, CAS, WE, CKE, ODT
VIX min, max	2.3 Differential Input Tests	DQS/DQS#, LDQS/LDQS#. UDQS/UDQS#, CK/CK#
Vlow	2.2 Single-Ended AC Tests, Data and Mask	DQ*, DM
Vmax(overshoot)	2.1 Single-Ended AC Input Tests, Address and Control	A0-A15, BA0-BA2, CS, RAS, CAS, WE, CKE, ODT
Vmax(overshoot)	2.2 Single-Ended AC Tests, Data and Mask	DQ*, DM
Vmin(overshoot)	2.1 Single-Ended AC Input Tests, Address and Control	A0-A15, BA0-BA2, CS, RAS, CAS, WE, CKE, ODT
Vmin(overshoot)	2.2 Single-Ended AC Tests, Data and Mask	DQ*, DM
VSEH	2.3 Differential Input Tests	DQS/DQS#, LDQS/LDQS#. UDQS/UDQS#, CK/CK#
VSEL	2.3 Differential Input Tests	DQS/DQS#, LDQS/LDQS#. UDQS/UDQS#, CK/CK#